PTO-1449

Information Disclosure Citation in an Application

Application No.	Applicant(s):		
10/735,956	Joel Hatsch et al.		
Docket Number	Group Art Unit	Filing Date	
068758.0151	2182	December 15, 2003	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
Mgn	1	3,757,098	09-04-73	Wright	235	175	05-12-72
	2	5,504,915	04-02-96	Rarick	395	800	08-05-93
	3	6,345,286	02-05-02	Dhong et al.	708	708	10-30-98

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
Mgn	4	P.J. Song, et al.; "Circuit and Architecture Trade-Offs for High-Speed Multiplication; IEEE Journal of Solid-State Circuits; New York, US, Vol. 26, No. 9, pp. 1184-1198	09-01-91
	5	Zhongde Wang, et al.; "An Architecture for Parallel Multipliers"; IEEE Comp. Soc., Press, US, vol. 1, pp. 403-407	11-1991
	6	J.V. Salmon et al.; "Syntactic translation and logic synthesis in Gatemap"; IEEE Proceedings E. Computers & Digital Techniques; Institution of Electrical Engineers, Stevenage, GB; vol. 136; No. 4, part E, pp. 321-328	07-01-89
	7	Dinesh Somasekhar et al.; "Differential Current Switch Logic: A Low Power DCVS Logic Family"; IEEE Journal of Solid-State Circuits; IEEE Inc., New York, Vol. 31, No. 7, pp. 981-991	07-10-96

EXAMINER	DATE CONSIDERED
	3/2005

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.